Referring to FIG. 1, FIG. 1 is a function block diagram of a phase lock loop 10 according to the present invention. The phase lock loop 10 comprises a frequency synthesizer 12, a first programmable divider 14, a modulator 16, a phase detector 18, a charging pump 20, a loop filter 22, ~~a voltage-controlled oscillator~~ an oscillating signal generator 24, and a frequency converter 26. In another preferred embodiment, the oscillating signal generator 24 may comprise a voltage-controlled oscillator (VCO) (not shown). In another preferred embodiment, the oscillating signal generator 24 may comprise a voltage-controlled oscillator (not shown) and a third frequency divider (not shown) coupled to an output of the voltage-controlled oscillator.

NM 1/7/08

Paragraph beginning on page ~~5~~ 4, at prenumbered line ~~3~~ 24, has been amended as follows:

The phase detector 18 is used to detect phases of the first comparison signal S_1 and a second comparison signal S_2 and output a corresponding current-controlled I/O signal S_{IO} in response to the phase difference between the two comparison signals S_1 and S_2. The charging pump 20 is used to receive the current-controlled I/O signal S_{IO} and accordingly output a corresponding control current I. The loop filter 22 filters the control current I to output a control voltage V to the voltage-controlled oscillator 24.

NM 1/7/08

Paragraph beginning on page 5, at prenumbered line ~~15~~ 11, has been amended as follows:

Provided that a carrier frequency of the RF signal substantially equals to a predetermined value, the first programmable divisor of the first programmable divider as well as the corresponding local oscillating frequency of the local oscillating signal are capable of being programmable-controlled. In other words, the ~~The~~ first programmable divisor M of the first programmable divider 14 is programmable-controlled ~~so~~, so as to prevent the occurrence of a spur frequency, besides the predetermined transmission frequency, in the RF signal due to the interfered local oscillating signal.

NM 1/7/08

Paragraph beginning on page 11, at prenumbered line 3, has been amended as follows:

The present invention provides a phase lock loop for receiving a baseband signal that has an input frequency and modulating the baseband signal to be a corresponding RF signal. The RF signal has a predetermined transmission frequency for transmitting. The phase lock loop comprises a frequency synthesizer, a first programmable divider, a modulator, ~~a voltage-controlled oscillator~~an oscillating signal generator, and a frequency converter. The first programmable divisor of the first programmable divider is programmable-controlled so as to prevent the occurrence of a spur frequency, besides the predetermined transmission frequency, in the RF signal due to the interfered local oscillating signal. By using the present invention, all channels of the GSM system, can select suitable local oscillating frequency, without causing the problem of lower output signal quality.